The Designer's Guide to Jitter in Ring Oscillators

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Springer

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Preface

This is a book for engineers concerned with jitter: the effects of noise visible in the time domain. The material presented will be helpful for work at both the system level and the circuit level:

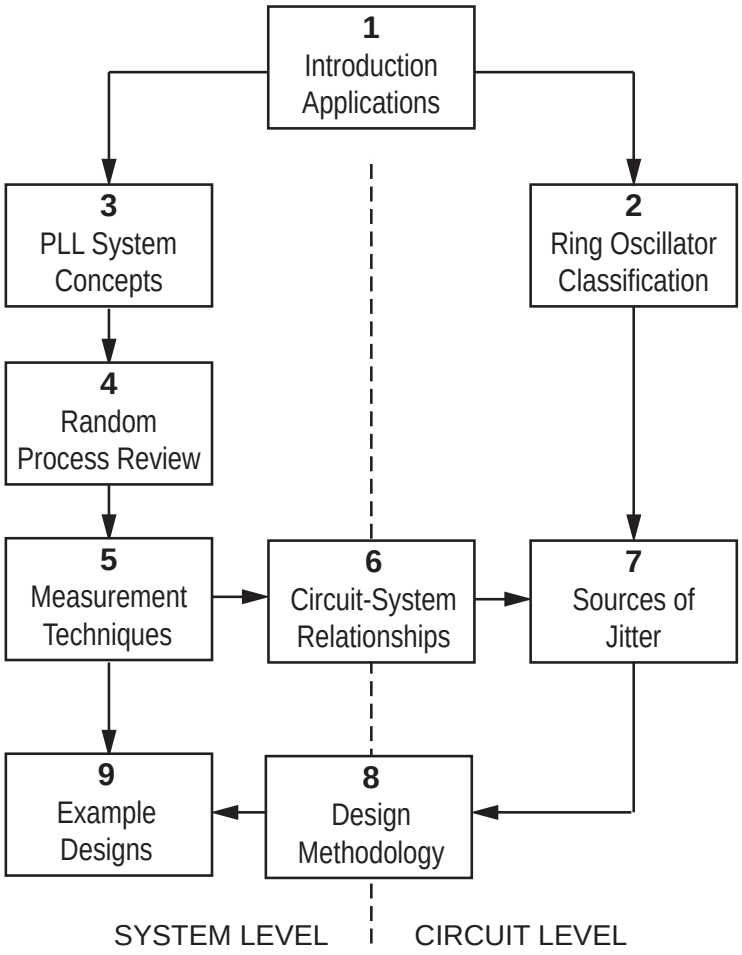
- At the system level, the challenge is to describe, specify, and measure time domain uncertainty and when necessary, relate jitter to phase noise specifications in the frequency domain.
- At the circuit level, the challenge is to design low noise circuitry within power, area, and process constraints so that ultimate performance meets system level requirements.

Throughout the book concepts are presented in the context of an engineering application requiring low jitter performance: the voltage controlled oscillator (VCO) used in a phase-locked loop (PLL). Techniques are presented for circuit-level design of low jitter delay elements for use in ring oscillators, as well as relating the circuit-level characteristics to system-level performance. Although the emphasis is on time-domain (jitter) measures of oscillator performance, a simple method of translating performance to frequency domain (phase noise) measures is presented as well.

Structure of this Book

This book is divided into nine chapters. The diagram on the following page shows the relationship between material in each chapter as well as placement in the system-level vs. circuit-level design hierarchy. Wherever possible, experimental verification is presented in the same chapter as the corresponding theoretical development, rather than being isolated in a separate chapter.

Chapter 1 begins as a bridge between the system and circuit levels, describing a range of applications for which jitter is a concern and beginning the exploration of the ring oscillator on the circuit level. Somewhat more emphasis is placed on clock recovery in serial data communication, the main



application for which this work was originally done. Chapter 1 also provides a brief overview of the different types of VCOs that are used in clock recovery PLLs, and establishes the need for an intuitive methodology to guide design for low-jitter ring VCOs.

Chapter 2 provides a classification of existing ring oscillator delay stage circuits according to signal type, output, and method of tuning. This classification scheme is organized from the circuit designer's perspective, covering most existing ring oscillator architectures and laying the foundation at the circuit level for the system level analysis techniques that will be developed to guide the designer in choosing among the options and tradeoffs in the ring oscillator VCO design process.

Chapter 3 introduces fundamental concepts for understanding phase, phase noise, and jitter, as well as their effect on the PLL. A review of fundamental PLL and phase noise concepts shows how VCO jitter is shaped by PLL loop dynamics to determine system-level jitter. After a brief introduction to jitter measurement techniques, several different system-level jitter and phase noise measures are specified which will be related by a mathematical framework to be described in Chapter 5.

Chapter 4 reviews the basic system-level concepts of random signals and noise used in the development of the mathematical framework of Chapter 5. It is meant as a review for the reader who has studied random signals or as an introduction for the circuit designer new to the area.

Chapter 5 covers the mathematical development of a technique for relating different jitter and phase noise measures introduced in Chapter 5. A key insight in this chapter is the definition of figures-of-merit, N_1 (frequency domain) and $\mathcal{K}$ (time domain), to describe jitter of the open-loop VCO. Knowledge of either N_1 or $\mathcal{K}$, together with the PLL loop dynamics, gives complete information on the system-level closed-loop jitter performance as measured in either the time or frequency domain. The technique is verified experimentally through measurements made on several existing PLLs and VCOs in both closed loop and open loop conditions.

The material in Chapter 6 begins building a "bridge" in the methodology necessary for circuit-level design to meet a required system-level specification. It is seen that the time domain figure-of-merit $\mathcal{K}$ is independent of both the ring frequency and number of stages, and thus can provide an intuitive link between circuit-level and system-level performance. This leads to a simple, general design methodology which flows naturally from the time-frequency domain relationships described in Chapter 5. Experimental results are presented verifying the concepts underlying the methodology.

Chapter 7 is concerned with circuit-level design of delay stages to realize a low-jitter ring VCO function. The jitter figure of merit $\mathcal{K}$, developed in Chapters 5 and 6, is applied to characterize jitter in delay stages designed in both CMOS and bipolar technologies. Explicit numerical relationships are developed relating noise sources to resulting jitter. Simulated and experimental results from several rings of different lengths demonstrate the applicability of this approach. Comparing the expressions for $\mathcal{K}$ in rings with results from other types of VCOs illuminates the relative merits of ring oscillators in terms of jitter performance.

Chapter 8 completes the "bridge" back to the system level from the circuit level, providing a summary of the entire methodology for the designer whose interest is circuit level design of a low jitter ring oscillator. Starting with desired jitter performance at the system level, expressed in either the time or frequency domain, the procedure gives explicit constraints on values of circuit elements.

As examples of the procedure in Chapter 8, the design of low jitter ring VCOs for both CMOS and bipolar PLLs is described in Chapter 9. Design

techniques for overcoming some of the inherent limitations of the ring architecture are discussed. Measured test results, incorporating the techniques of Chapter 7 are presented showing good agreement to the design methodology's numerical predictions.

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