

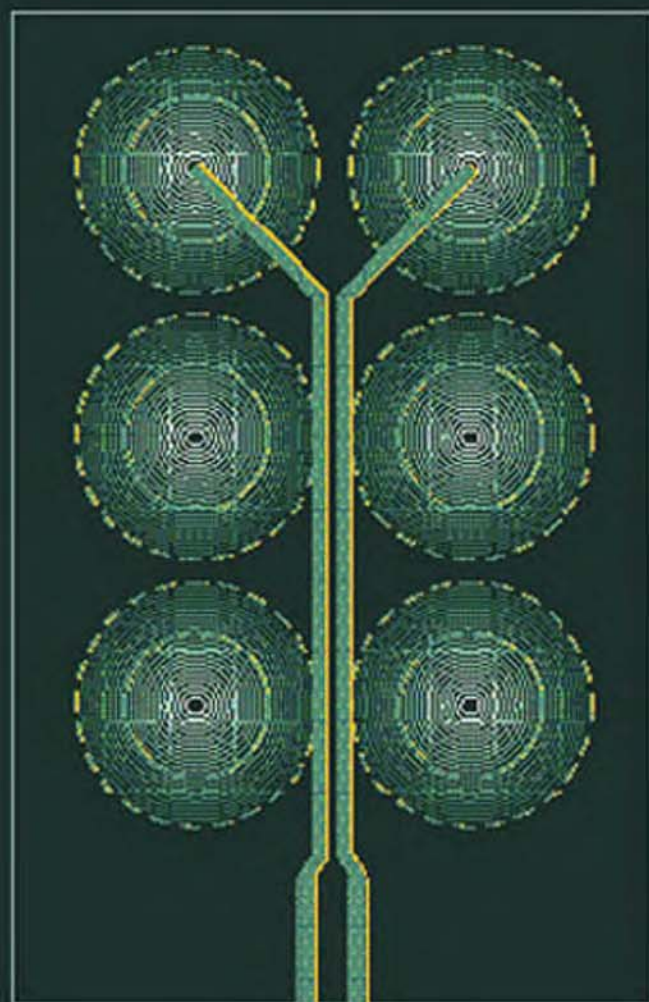
Brought to You by

Team LiB

The logo for Team LiB features the text "Team LiB" in a bold, yellow, sans-serif font with a black outline. The text is centered within a blue, swoosh-like graphic that curves around the top and right sides of the letters.

Like the book? Buy it!

STEPHEN C. THIERAUF



HIGH-SPEED
CIRCUIT BOARD
SIGNAL INTEGRITY

High-Speed Circuit Board Signal Integrity

For a listing of recent titles in the *Artech House Microwave Library*,
turn to the back of this book.

High-Speed Circuit Board Signal Integrity

Stephen C. Thierauf



Artech House, Inc.
Boston • London
www.artechhouse.com

Library of Congress Cataloguing-in-Publication Data

A catalog record for this book is available from the U.S. Library of Congress.

British Library Cataloguing in Publication Data

A catalog record for this book is available from the British Library.

Cover design by Igor Valdman

© 2004 ARTECH HOUSE, INC.
685 Canton Street
Norwood, MA 02062

All rights reserved. Printed and bound in the United States of America. No part of this book may be reproduced or utilized in any form or by any means, electronic or mechanical, including photocopying, recording, or by any information storage and retrieval system, without permission in writing from the publisher.

All terms mentioned in this book that are known to be trademarks or service marks have been appropriately capitalized. Artech House cannot attest to the accuracy of this information. Use of a term in this book should not be regarded as affecting the validity of any trademark or service mark.

International Standard Book Number: 1-58053-131-8

10 9 8 7 6 5 4 3 2 1

To Ann, Christopher, and Kevin

Contents

Preface	<i>xiii</i>
CHAPTER 1	
Characteristics and Construction of Printed Wiring Boards	1
1.1 Introduction	1
1.2 Unit System	1
1.3 PWB Construction	2
1.3.1 Resins	3
1.3.2 Alternate Resin Systems	3
1.3.3 Reinforcements	5
1.3.4 Variability in Building Stackups	6
1.3.5 Mixing Laminate Types	7
1.4 PWB Traces	7
1.4.1 Copper Cladding	8
1.4.2 Copper Weights and Thickness	9
1.4.3 Plating the Surface Traces	9
1.4.4 Trace Etch Shape Effects	9
1.5 Vias	10
1.5.1 Via Aspect Ratio	13
1.6 Surface Finishes and Solder Mask	14
1.7 Summary	14
References	15
CHAPTER 2	
Resistance of Etched Conductors	17
2.1 Introduction	17
2.2 Resistance at Low Frequencies	17
2.3 Loop Resistance and the Proximity Effect	20
2.3.1 Resistance Matrix	21
2.3.2 Proximity Effect	22
2.4 Resistance Increase with Frequency: Skin Effect	24
2.5 Hand Calculations of Frequency-Dependent Resistance	27
2.5.1 Return Path Resistance	28
2.5.2 Conductor Resistance	28
2.5.3 Total Loop Resistance	29
2.6 Resistance Increase Due to Surface Roughness	29
2.7 Summary	30

References	30
CHAPTER 3	
Capacitance of Etched Conductors	31
3.1 Introduction	31
3.2 Capacitance and Charge	31
3.2.1 Dielectric Constant	32
3.3 Parallel Plate Capacitor	33
3.4 Self and Mutual Capacitance	35
3.5 Capacitance Matrix	37
3.6 Dielectric Losses	39
3.6.1 Reactance and Displacement Current	40
3.6.2 Loss Tangent	40
3.6.3 Calculating Loss Tangent and Conductance G	41
3.7 Environmental Effects on Laminate ϵ_r and Loss Tangent	43
3.7.1 Temperature Effects	44
3.7.2 Moisture Effects	44
3.8 Summary	45
References	45
CHAPTER 4	
Inductance of Etched Conductors	47
4.1 Introduction	47
4.2 Field Theory	47
4.2.1 Permeability	48
4.2.2 Inductance	48
4.2.3 Internal and External Inductance	49
4.2.4 Partial Inductance	49
4.2.5 Reciprocity Principle and Transverse Electromagnetic Mode	50
4.3 Circuit Behavior of Inductance	51
4.3.1 Inductive Voltage Drop	53
4.3.2 Inductive Reactance	54
4.4 Inductance Matrix	55
4.4.1 Using the Reciprocity Principle to Obtain the Inductance Matrix from a Capacitance Matrix	55
4.5 Mutual Inductance	55
4.5.1 Coupling Coefficient	56
4.5.2 Beneficial Effects of Mutual Inductance	57
4.5.3 Deleterious Effects of Mutual Inductance	59
4.6 Hand Calculations for Inductance	60
4.6.1 Inductance of a Wire Above a Return Plane	60
4.6.2 Inductance of Side-by-Side Wires	61
4.6.3 Inductance of Parallel Plates	61
4.6.4 Inductance of Microstrip	63
4.6.5 Inductance of Stripline	63
4.7 Summary	64
References	65

CHAPTER 5

Transmission Lines	67
5.1 Introduction	67
5.2 General Circuit Model of a Lossy Transmission Line	67
5.2.1 Relationship Between ωL and R	70
5.2.2 Relationship Between ωC and G	70
5.3 Impedance	71
5.3.1 Calculating Impedance	72
5.4 Traveling Waves	73
5.4.1 Propagation Constant	74
5.4.2 Phase Shift, Delay, and Wavelength	75
5.4.3 Phase Constant at High Frequencies When R and G Are Small	78
5.4.4 Attenuation	79
5.4.5 Neper and Decibel Conversion	80
5.5 Summary and Worked Examples	82
References	86

CHAPTER 6

Return Paths and Power Supply Decoupling	87
6.1 Introduction	87
6.2 Proper Return Paths	87
6.2.1 Return Paths of Ground-Referenced Signals	89
6.2.2 Stripline	90
6.3 Stripline Routed Between Power and Ground Planes	90
6.3.1 When Power Plane Voltage Is the Same as Signal Voltage	90
6.3.2 When Power Plane Voltage Differs from Signal Voltage	93
6.3.3 Power System Inductance	94
6.4 Split Planes, Motes, and Layer Changes	95
6.4.1 Motes	95
6.4.2 Layer Changes	98
6.5 Connectors and Dense Pin Fields	98
6.5.1 Plane Perforation	99
6.5.2 Antipads	99
6.5.3 Nonfunctional Pads	102
6.5.4 Guidelines for Routing Through Dense Pin Fields	103
6.6 Power Supply Bypass/Decoupling Capacitance	105
6.6.1 Power Supply Integrity	106
6.6.2 Distributed Power Supply Interconnect Model	110
6.7 Connecting to Decoupling Capacitors	112
6.7.1 Via Inductance	112
6.8 Summary	114
References	115

CHAPTER 7

Serial Communication, Loss, and Equalization	117
7.1 Introduction	117
7.2 Harmonic Contents of a Data Stream	117

7.2.1	Line Spectra	119
7.2.2	Combining Harmonics to Create a Pulse	120
7.2.3	The Fourier Integral	122
7.2.4	Rectangular Pulses with Nonzero Rise Times	123
7.3	Line Codes	125
7.4	Bit Rate and Data Rate	126
7.5	Block Codes Used in Serial Transmission	128
7.6	ISI	130
7.6.1	Dispersion	130
7.6.2	Lone 1-Bit Pattern	131
7.7	Eye Diagrams	132
7.8	Equalization and Preemphasis	134
7.8.1	Preemphasis	134
7.8.2	Passive Equalizers	137
7.8.3	Passive RC Equalizer	139
7.9	DC-Blocking Capacitors	140
7.9.1	Calculating the Coupling Capacitor Value	142
7.10	Summary	145
	References	146
CHAPTER 8		
	Single-Ended and Differential Signaling and Crosstalk	149
8.1	Introduction	149
8.2	Odd and Even Modes	149
8.2.1	Circuit Description of Odd and Even Modes	150
8.2.2	Coupling Coefficient	153
8.2.3	Stripline and Microstrip Odd- and Even-Mode Timing	155
8.2.4	Effects of Spacing on Impedance	157
8.3	Multiconductor Transmission Lines	158
8.3.1	Bus Segmentation for Simulation Purposes	159
8.3.2	Switching Behavior of a Wide Bus	160
8.3.3	Simulation Results for Loosely Coupled Lines	161
8.3.4	Simulation Results for Tightly Coupled Lines	162
8.3.5	Data-Dependent Timing Jitter in Multiconductor Transmission Lines	164
8.4	Differential Signaling, Termination, and Layout Rules	165
8.4.1	Differential Signals and Noise Rejection	165
8.4.2	Differential Impedance and Termination	166
8.4.3	Reflection Coefficient and Return Loss	170
8.4.4	PWB Layout Rules When Routing Differential Pairs	172
8.5	Crosstalk	173
8.5.1	Coupled-Line Circuit Model	175
8.5.2	NEXT and FEXT Coupling Factors	177
8.5.3	Using K_b to Predict NEXT	178
8.5.4	Using K_r to Predict FEXT	179
8.5.5	Guard Traces	179
8.5.6	Crosstalk Worked Example	180

8.5.7 Crosstalk Summary	182
8.6 Summary	182
References	183
CHAPTER 9	
Characteristics of Printed Wiring Stripline and Microstrips	185
9.1 Introduction	185
9.2 Stripline	185
9.2.1 Time of Flight	186
9.2.2 Impedance Relationship Between Trace Width, Thickness, and Plate Spacing	187
9.2.3 Mask Biasing to Obtain a Specific Impedance	189
9.2.4 Hand Calculation of Z_0	189
9.2.5 Stripline Fabrication	191
9.3 Microstrip	193
9.3.1 Exposed Microstrip	194
9.3.2 Solder Mask and Embedded Microstrip	196
9.4 Losses in Stripline and Microstrip	197
9.4.1 Dielectric Loss	199
9.4.2 Conductor Loss	199
9.5 Microstrip and Stripline Differential Pairs	201
9.5.1 Broadside Coupled Stripline	201
9.5.2 Edge-Coupled Stripline	204
9.5.3 Edge-Coupled Microstrip	205
9.6 Summary	206
References	207
CHAPTER 10	
Surface Mount Capacitors	209
10.1 Introduction	209
10.2 Ceramic Surface Mount Capacitors	209
10.2.1 Dielectric Temperature Characteristics Classification	209
10.2.2 Body Size Coding	211
10.2.3 Frequency Response	212
10.2.4 Inductive Effects: ESL	214
10.2.5 Dielectric and Conductor Losses: ESR	215
10.2.6 Leakage Currents: Insulation Resistance	218
10.2.7 Electrical Model	219
10.2.8 MLCC Capacitor Aging	220
10.2.9 Capacitance Change with DC Bias and Frequency	221
10.2.10 MLCC Usage Guidelines	222
10.3 SMT Tantalum Capacitors	223
10.3.1 Body Size Coding	223
10.3.2 Frequency Response	224
10.3.3 Electrical Model	225
10.3.4 Aging	225
10.3.5 Effects of DC Bias, Temperature, and Relative Humidity	225

10.3.6	Failure of Tantalum Capacitors	226
10.3.7	ESR and Self Heating: Voltage and Temperature Derating	227
10.3.8	Usage Guidelines	227
10.4	Replacing Tantalum with High-Valued Ceramic Capacitors	228
	References	230
	Appendix: Conversion Factors	231
	About the Author	233
	Index	235