IEEE Press Editorial Board

Roger F. Hoyt, Editor-in-Chief

J. B. Anderson S. Furui P. Laplante
P. M. Anderson A. H. Haddad M. Padgett
M. Eden R. Herrick W. D. Reeve
M. E. El-Hawary S. Kartalopoulos G. Zobrist
D. Kirk

Kenneth Moore, Director of IEEE Press John Griffin, Acquisition Editor Marilyn G. Catis, Assistant Editor Denise Phillip, Production Editor

IEEE Electromagnetic Compatibility Society, Sponsor EMC-S Liaison to IEEE Press, Hugh Denny

Cover design: William T. Donnelly, WT Design

Technical Reviewers

Daryl Gerke, P.E., Kimmel Gerke Associated, Ltd.
William H. Hubbard, Purdue University
Elya B. Joffe, K.T.M. Project Engineering, Ltd.
William Kimmel, Kimmel Gerke Associated, Ltd.
W. Michael King
Norm Violette, Violette Engineering Corp.

Books of Related Interest from IEEE Press

PRINTED CIRCUIT BOARD DESIGN TECHNIQUES FOR EMC COMPLIANCE

Mark I. Montrose

1996 Cloth 256 pp

ISBN 0-7803-1131-0

CAPACITIVE SENSORS: Design and Applications

Larry Baxter

1997

Cloth 320 pp

ISBN 0-7803-1130-2

EMC AND THE PRINTED CIRCUIT BOARD

Design, Theory, and Layout Made Simple

Mark I. Montrose

Montrose Compliance Services, Inc.

IEEE Electromagnetic Compatibility Society, Sponsor

IEEE Press Series on Electronics Technology Robert Herrick, Series Editor



The Institute of Electrical and Electronics Engineers, Inc., New York



A JOHN WILEY & SONS, INC., PUBLICATION

New York • Chichester • Weinheim • Brisbane • Singapore • Toronto

© 1999 THE INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, INC. 3 Park Avenue. 17th Floor, New York, NY 10016-5997 All rights reserved.

No part of this publication may be reproduced, stored in a retrieval system, or transmitted in any form or by any means, electronic, mechanical, photocopying, recording, scanning or otherwise, except as permitted under Sections 107 and 108 of the 1976 United States Copyright Act, without either the prior written permission of the Publisher, or authorization through payment of the appropriate per-copy fee to the Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923, (978) 750-8400, fax 0788 750-4744, Requests to the Publisher for permission should be addressed to the Permissions Department, John Wiley & Sons, Inc., 605 Third Avenue, New York, NY 10158-0012, (212) 850-6011, fax (212) 850-6008, E-mail: PERMREQ & WILEY COM.

For ordering and customer service, call 1-800-CALL-WILEY, Wiley-Interscience-IEEE ISBN 0-7803-4703-X

Printed in the United States of America. 10^{-9} 8 $\stackrel{?}{=}$ 6 5 4

Library of Congress Cataloging-in-Publication Data

Montrose, Mark 1.

EMC and the printed circuit board : design, theory, and layout made simple / Mark 1. Montrose.

CIP

p. cm. — (IEEE Press series on electronics technology)
"IEEE Electromagnetic Compatibility Society, sponsor."
Includes bibliographical references and index.
ISBN 0-7803-4703-X (alk. paper)
1. Printed circuits—Design and construction. 2. Electromagnets

1. Printed circuits—Design and construction. 2. Electromagnetic compatibility. I. IEEE Electromagnetic Compatibility Society. II. Title. III. Series.

TK7868.P7M65 1998
621.3815'31—dc21 98-35408

To my family

Margaret,

Maralena,

and Matthew

1

eface

md

PREFACE xiii

ACKNOWLEDGMENTS xvii

CHAPTER 1 EMC FUNDAMENTALS 1

- 1.1 Fundamental Definitions 2
- 1.2 EMC Concerns for the Design Engineer 4
 - 1.2.1 Regulations 4
 - 1.2.2 RFI 4
 - 1.2.3 Electrostatic discharge (ESD) 5
 - 1.2.4 Power disturbances 5
 - 1.2.5 Self-compatibility 6
- 1.3 The Electromagnetic Environment 6
- 1.4 The Need to Comply (A Brief History of EMI) 9
- Potential EMI/RFI Emission Levels for Unprotected Products 12
- 1.6 Methods of Noise Coupling 12
- 1.7 Nature of Interference 16
 - 1.7.1 Frequency and Time (à la Fourier: time domain ⇔ frequency domain) 17
 - 1.7.2 Amplitude 18
 - 1.7.3 Impedance 18
 - 1.7.4 Dimensions 18
- 1.8 PCBs and Antennas 18
- 1.9 Causes of EMI—System Level 19
- 1.10 Summary for Control of Electromagnetic Radiation 20 References 21

CHAPTER 2 EMC INSIDE THE PCB 23

- 2.1 EMC and the PCB 23
 - 2.1.1 Wires and PCB-traces 25
 - 2.1.2 Resistors 25
 - 2.1.3 Capacitors 26
 - 2.1.4 Inductors 26
 - 2.1.5 Transformers 27
- 2.2 Theory of Electromagnetics (Made Simple) 28
- Relationship Between Electric and Magnetic Sources (Made Simple) 30
- 2.4 Maxwell Simplified-Further Still 34
- 2.5 Concept of Flux Cancellation (Flux Minimization) 37
- 2.6 Skin Effect and Lead Inductance 39
- 2.7 Common-Mode and Differential-Mode Currents 41
 - 2.7.1 Differential-mode currents 42
 - 2.7.2 Differential-mode radiation 42
 - 2.7.3 Common-mode currents 44
 - 2.7.4 Common-mode radiation 46
 - 2.7.5 Conversion between differential and common mode 46
- 2.8 Velocity of Propagation 47
- 2.9 Critical Frequency (λ/20) 49
- 2.10 Fundamental Principles and Concepts for Suppression of RF Energy 49
 - 2.10.1 Fundamental principles 49
 - 2.10.2 Fundamental concepts 49
- 2.11 Summary 51 References 52

CHAPTER 3 COMPONENTS AND EMC 53

- 3.1 Edge Rate 53
- 3.2 Input Power Consumption 56
- 3.3 Clock Skew 58
 - 3.3.1 Duty cycle skew 59
 - 3.3.2 Output-to-output skew 59
 - 3.3.3 Part-to-part skew 60
- 3.4 Component Packaging 60
- 3.5 Ground Bounce 65
- 3.6 Lead-to-Lead Capacitance 69
- 3.7 Grounded Heatsinks 70
- 3.8 Power Filtering for Clock Sources 74
- 3.9 Radiated Design Concerns for Integrated Circuits 76
- 3.10 Summary for Radiated Emission Control—Component Level 78 References

CHAPTER 4 IMAGE PLANES 81

- 4.1 Overview 81
- 4.2 5/5 Rule 83
- 4.3 How Image Planes Work 84
 - 4.3.1 Inductance 84
 - 4.3.2 Partial inductance 85
 - 4.3.3 Mutual partial inductance 86
 - 4.3.4 Image plane implementation and concept 88
- 4.4 Ground and Signal Loops (Not Eddy Currents) 91
 - 4.4.1 Loop area control 92
- 4.5 Aspect Ratio—Distance Between Ground Connections 95
- 4.6 Image Planes 97
- 4.7 Image Plane Violations 99
- 4.8 Layer Jumping-Use of Vias 102
- 4.9 Split Planes 104
- 4.10 Partitioning 106
 - 4.10.1 Functional subsystems 106
 - 4.10.2 Quiet areas 106
- 4.11 Isolation and Partitioning (Moating) 107
 - 4.11.1 Method 1: Isolation 108
 - 4.11.2 Method 2: Bridging 108
- 4.12 Interconnects and RF Return Currents 112
- 4.13 Layout Concerns for Single- and Double-Sided Boards 114
 - 4.13.1 Single-sided PCBs 115
 - 4.13.2 Double-sided PCBs 116
 - 4.13.3 Symmetrically placed components 116
 - 4.13.4 Asymmetrically placed components 118
- 4.14 Gridded Ground System 119
- 4.15 Localized Ground Planes 120
 - 4.15.1 Digital-to-analog partitioning 122
- 4.16 Summary 123

References 124

CHAPTER 5 BYPASSING AND DECOUPLING 125

- 5.1 Review of Resonance 126
 - 5.1.1 Series resonance 127
 - 5.1.2 Parallel resonance 128
 - 5.1.3 Parallel C—Series RL resonance (antiresonant circuit) 128
- 5.2 Physical Characteristics 129
 - 5.2.1 Impedance 129
 - 5.2.2 Energy storage 131
 - 5.2.3 Resonance 132
 - 5.2.4 Benefits of power and ground planes 134

- 5.3 Capacitors in Parallel 136
- 5.4 Power and Ground Plane Capacitance 138
 5.4.1 Buried capacitance 141
 5.4.2 Calculating power and ground plane capacitance 142
- 5.5 Lead-Length Inductance 143
- 5.6 Placement 144
 5.6.1 Power planes 144
 5.6.2 Decoupling capacitors 144
- 5.7 Selection of a Decoupling Capacitor 1485.7.1 Calculating capacitor values (wave-shaping) 149
- 5.8 Selection of Bulk Capacitors 152
- 5.9 Designing a Capacitor Internal to a Component's Package 155
- 5.10 Vias and Their Effects in Solid Power Planes 157 References 158

CHAPTER 6 TRANSMISSION LINES 159

- 6.1 Overview on Transmission Lines 159
- 6.2 Transmission Line Basics 162
- 6.3 Transmission Line Effects 163
- 6.4 Creating Transmission Lines in a Multilayer PCB 165
- 6.5 Relative Permittivity (Dielectric Constant) 166 6.5.1 How losses occur within a dielectric 169
- 6.6 Routing Topologies 171
 - 6.6.1 Microstrip topology 171
 - 6.6.2 Embedded microstrip topology 172
 - 6.6.3 Single stripline topology 174
 - 6.6.4 Dual stripline topology 175
 - 6.6.5 Differential microstrip and stripline 177
- 6.7 Routing Concerns 178
- 6.8 Capacitive Loading 180 References 182

CHAPTER 7 SIGNAL INTEGRITY AND CROSSTALK 185

- 7.1 Need for Signal Integrity 185
- 7.2 Reflections and Ringing 188
 - 7.2.1 Identification of signal distortion 1917.2.2 Conditions that create ringing 192
- 7.3 Calculating Trace Lengths (Electrically Long Traces) 195
- 7.4 Loading Due to Discontinuities 200
- 7.5 RF Current Distribution 202

- 7.6 Crosstalk 203
 7.6.1 Units of measurement—Crosstalk 206
 7.6.2 Design techniques to prevent crosstalk 207
- 7.7 The 3-W Rule 210 References 212

CHAPTER 8 TRACE TERMINATION 215

- 8.1 Transmission Line Effects 216
- 8.2 Termination Methodologies 217
 - 8.2.1 Source termination 221
 - 8.2.2 Series termination 221
 - 8.2.3 End termination 226
 - 8.2.4 Parallel termination 227
 - 8.2.5 Thevenin network 230
 - 8.2.6 RC network 234
 - 8.2.7 Diode network 236
- 8.3 Terminator Noise and Crosstalk 237
- 8.4 Effects of Multiple Terminations 239
- 8.5 Trace Routing 241
- 8.6 Bifurcated Lines 243
- 8.7 Summary—Termination Methods 244
 References 245

CHAPTER 9 GROUNDING 247

- 9.1 Reasons for Grounding-An Overview 247
- 9.2 Definitions 247
- 9.3 Fundamental Grounding Concepts 249
- 9.4 Safety Ground 253
- 9.5 Signal Voltage Referencing Ground 254
- 9.6 Grounding Methods 255
 - 9.6.1 Single-point grounding 256
 - 9.6.2 Multipoint grounding 259
 - 9.6.3 Hybrid or selective grounding 261
 - 9.6.4 Grounding analog circuits 261
 - 9.6.5 Grounding digital circuits 262
- 9.7 Controlling Common-Impedance Coupling Between Traces 262
 - 9.7.1 Lowering the common-impedance path 262 9.7.2 Avoiding a common-impedance path 264
- 9.8 Controlling Common-Impedance Coupling in Power and Ground 266
- 9.9 Ground Loops 268
- 9.10 Resonance in Multipoint Grounding 271

xii

Contents

9.11 Field Transfer Coupling of Daughter Cards to Card Cage 273
9.12 Grounding (I/O Connector) 277
References 277

GLOSSARY 279

BIBLIOGRAPHY 287

APPENDIX

A The Decibel 291

B Fourier Analysis 294

C Conversion Tables 298

D International EMC Requirements 302

INDEX 317

ABOUT THE AUTHOR 325

Preface

EMC and the Printed Circuit Board: Design, Theory, and Layout Made Simple is a companion book to Printed Circuit Board Design Techniques for EMC Compliance. When used together, these two books cover all aspects of a PCB design as it relates to both time and frequency domain issues. One must be cognizant that if a PCB does not work as intended in the time domain, frequency domain concerns become irrelevant, especially compliance to international EMC requirements. Time and frequency domain aspects must be considered together.

The intended audience for this book is the same as that for *Printed Circuit Board Design Techniques for EMC Compliance:* those involved in logic design and PCB layout; test engineers and technicians; those working in the areas of mechanical, manufacturing, production, and regulatory compliance; EMC consultants: and management responsible for overseeing a hardware engineering design team.

Regardless of the engineer's specialty, a design team must come up with a product that not only can be manufactured in a reasonable time period, but will also minimize cost during design, test, integration, and production. Frequently, more emphasis is placed on functionality to meet a marketing specification than on the need to meet legally mandated EMC and product safety requirements. If a product fails to meet compliance tests, redesign or rework may be required. This redesign significantly increases costs, which include, but are not limited to engineering manpower (along with administrative overhead), new PCB layout and artwork, prototyping material, system integration and testing, purchase of new components for quick delivery (very expensive), new in-circuit test fixtures, and documentation. These costs are in addition to loss of market share, delayed shipment, loss of customer faith in the company (goodwill), drop in stock price, anxiety attacks, and many other issues. Personal experience as a consultant has allowed me the opportunity to witness these events several times with small startup companies.

My main focus as a consultant is to assist and advise in the design of high-technology products at minimal cost. Implementing suppression techniques into the PCB design saves money, enhances performance, increases reliability, and achieves first-time compliance with emissions and immunity requirements, in addition to having the product function as desired.

Working in this industry has allowed me to participate in state-of-the-art designs as we move into the future. Although my focus is on technology of the future, one cannot